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Investigation of Electromagnetic Interference in Cmos Power Distribution Networks.

M.Lakshminarasimhacharyulu[1],.Murthy sarma[2],K.Lal kishore[3]

Research scholar,JNTUH&Professor GPCET, Kurnool[1].
Professor and HOD in BVCE odalarevu [2].
Vicechancellor , JNTUA[3]

Abstract— ***EM1 noise reduction is generally accomplished by three means: suppression of noise source, isolation of noise coupling path, and filter shielding. In this paper, another means of EMI noise reduction is proposed is Simultaneous switching noise (SSN) has become an important issue for generation of EMI effect in the design of the internal on chip power distribution networks in current very large scale integration/ultra large scale integration circuits. An inductive model is used to characterize the power supply rails when a transient current is generated by simultaneously switching the on-chip registers and logic gates in a synchronous CMOS VLSI/ULSI circuit. An analytical expression characterizing the SSN voltage is presented here based on a lumped inductive-resistive-capacitive model. The peak value of the SSN voltage based on this analytical expression is within 10% as compared to SPICE simulations. Design constraints at both the circuit and layout levels are also discussed based on minimizing the effects of the peak value of the SSN voltage.***

Key words—Integrated circuit interconnection, on-chip inductance, power distribution network, simultaneous switching noise.

INTRODUCTION

For predicting the EMI behavior of an integrated circuit it is necessary to perform an di/dt-analysis. For carrying out such a dynamic current analysis Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a circuit malfunction due to the distortion of the signal waveform [1]. According to this definition, a signal with good integrity presents: (i) voltage values at required levels and (ii) level transitions at required times.Various signal integrity problems have been studied for high-speed gigahertz nanometer System-on- Chip . The most important ones are: (a) crosstalk (signal distortion due to cross coupling effects betweensignals)[2,3]; (b) overshoot/undershoot (momentarily signal rising/decreasing above/below the power supply voltage (VDD) and ground (VSS) lines [4,5]; (c) reflection (echoing back a portion of a signal, at high- frequency circuits, where interconnections behave as transmission lines); (d) electromagnetic interference – EMI (resulting from antenna properties) [6,7]; (e) power-supply noise [8,9]; and (f) signal skew (delay in arrival time to different receivers) [10-12]. For consider the specific CMOS design it is absolutely necessary to do at first an extraction of the parasitic elements of the power supply lines. The parasitic elements in combination with the supply currents cause voltage drops on the supply lines. The static currents cause so called IR-drops at the resistors and the dynamic currents cause voltage drops V_L=L di/dt at the inductors. This could be validated by performing a circuit simulation of a CMOS gate which is connected to VDD via a supply line. The values for the inverter as well as for the line were taken from nanometer technology process. The trend of next generation integrated circuit (IC) technology is toward higher speeds and densities. The total capacitive load associated with the internal circuitry is there-fore increasing in both current and next generation very large scale integration (VLSI) circuits [13]–[15]. As the operating frequency increases, the average on-chip current required to charge (and discharge)these capacitances also increases, while the time during which the current being switched decreases. Therefore, a large change in the total on-chip current occurs within a short period of time. The primary sources of the current surges are the input/output (I/O) drivers and the internal logic circuitry, particularly those gates that switch close in time to the clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power supply network [16], which is called simultaneous switching noise (SSN) or delta-I noise. Most existing research on SSN has concentrated on the transient power noise caused by the current through the inductive bonding wires at the I/O drivers [17]–[21]. However, SSN originating from the internal circuitry is becoming an important issue in the design of very deep sub micrometer (VDSM) high-performance microprocessors [15], [22]. This increased importance can be attributed to fast clock rates, large on-chip switching activities, and large on-chip current, all of which are increasingly common characteristics of a VDSM synchronous inte- grated circuit. For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach 20 W/cm [23], [24], a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2 V power supply in a 0.1 m CMOS technology. Assuming that the current is uniformly distributed along a 1-cm-

wide and 1- m-thick Al-Cu interconnect plane, the average current density is approximately 1.63 mA/ m . For a standard mesh structured power distribution network, the current density is even greater than 1.63mA/ m . For a 1-mm-long power bus line with a parasitic inductance of 2 nH/cm [25], if the edge rate of the current signal is on the order of an overly conservative nanosecond, the amplitude of the noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS circuits. Therefore, on-chip SSN has become an important issue in VDSMintegratedcircuits.On-chipSSNaffectsthe signaldelay, creating delay uncertainty since the power supply level tempo- rally changes the local drive current [26]. Furthermore, logic malfunctions may be created and excess power may be dis- sipated due to faulty switching if the power supply fluctua- tions are sufficiently large [27], [28]. On-chip SSN must there- fore be controlled or minimized in high-performance integrated circuits.

An analytical expression characterizing the on-chip SSN voltage is presented here based on a lumped model characterizing the on-chip power supply rails rather other a single inductor to model a bonding wire. The MOS transistors are characterized by the th power law model [29], which is a more accurate device model than the Shichman–Hodges model for short-channel devices [30]. The SSN voltage predicted by the analytical expression is compared to SPICE. The waveform describing the SSN voltage is quite close to the waveform obtained from SPICE simulation. The peak value of the SSN is within 10% of SPICE. Circuit-level design constraints, such as the number of simultaneously switching logic gates connected to the same power supply rail, the drive current of the logic gates, the input transition time, and the magnitude of the power supply are related to the peak value of the SSN. For a specific parasitic inductive-resistive-capacitive impedance of the power supply rails,the analytical expressions presented here provide guidelines for designing the on-chip power distribution network. An analytical expression of the on-chip SSN voltage is de- scribed in Section II. A discussion of the dependence of the on-chip SSN voltage on the load capacitance, and related circuit and layout level constraints are presented in Section III followed by some concluding remarks in Section IV.

II. SIMULTANEOUS SWITCHING NOISE VOLTAGE

The power supply in high complexity CMOS circuits should provide sufficient current to support the average and peak power demand within all parts of an integrated circuit. An inductive, capacitive, and resistive model is used in this section to characterize the power supply rails when a transient current is generated by simultaneous switching of the on-chip registers and logic gates within a synchronous CMOS circuit. The short-channel MOS transistors are modeled as nonlinear devices and characterized by the th power law model, which is more accurate than the alpha power law model in both the linear region and the saturation region [26]. A CMOS logic gate in this discussion is modeled as a CMOS inverter. The power supply rail is characterized by a lumped model. The input signal is assumed to be a fast ramp.

assumption of a fast ramp input signal [31].

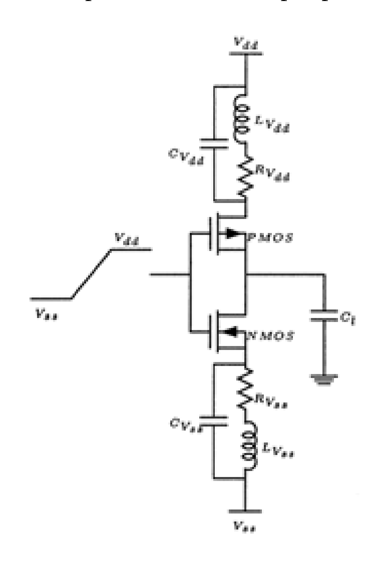


Fig. 1. An equivalent circuit for analyzing the SSN of an on-chip CMOS inverter

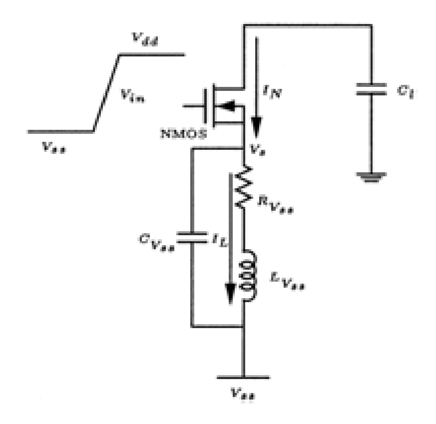


Fig. 2. SSN within a ground rail.

Theequivalent circuit depicted in Fig. 1 is used to characterize the SSN voltage on the power supply rails. The current through the PMOS transistor with a rising input signal, i.e., the short-circuit current, is neglected in this discus- sion when determining the SSN voltage on a ground rail based on the assumption of a fast ramp input signal [31]. The equivalent circuit therefore simplifies to the circuit shown in Fig. 2. and are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is for (1) After the input voltage reaches , the NMOS transistor turns ON and begins to operate in the saturation region.

It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed. The current through the NMOS transistor (2), the parasitic inductance ( ), and the SSN voltage ( ) are given, respectively, as

$$v_{in} = \frac{t}{\tau_T} v_{dd} \quad \text{for} \quad 0 \le t \le \tau_T \text{ ------(1)}$$

I_N = $B_n(V_{in}-V_{TN}-V_s)^n$-------------------------- (2)

V_s=R V_{ss} I_L+LV_{ss}(dI_L/dt)------------------------(3)

I_l=I_N.CV_{ss}(dV_s/dt) ------------------------------- (4)

Assuming that the magnitude of is small as compared to , can be approximated as

I_N≈$B_n(V_{in}-V_{TN})^n$-(dI_N/dV_{gs})V_s------------ (5)

Rewriting (5)

F_1=dI_N/dV_{GS}= n$B_n(V_{in}-V_{TN}-V_s)^{n-1}$ .... (6)

is a function of , i.e., for the case of an inverter. In order to simplify the derivation, is approximated using equal to 0.5 . Combining (4) –(6)F_1 is a function of V_{GS}

$L_{Vss}C_{Vss}(d^2V_s/dt^2)+(Rv_{ss}C_{Vss}+L_{Vss}f_1)(dV_s/dt)+(R_{Vss}f_1+1)V_s \cong R\, V_{ss}B_n(V_{in}-V_{TN})^n+L_{Vss}\, d/dt[B_n(V_{in}-V_{TN})^n]$----- (7)

1st term of LHS in eq(7)neglected and rest of two terms leads to $(Rv_{ss}\ C_{Vss}+L_{Vss}\ f_1)(dV_s/dt)+(R_{Vss}f_1+1)V_s \cong R\ V_{ss}B_nV^n_{dd}(t/T_r-V_n)^n+L\ V_{ss}B_nV^n_{dd}/T_r[(t/T_r-V_n)^{n-1}$--------------(8)

where .No closed form solution of this differential equation exists due to the non integer value of and In order to derive an analytical expression for the differential equation, and are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%

$$\xi^n = a_0 + a_1\xi + a_2\xi^2 + a_3\xi^3 + a_4\xi^4 + a_5\xi^5$$

$$\xi^{n-1} = b_0 + b_1\xi + b_2\xi^2 + b_3\xi^3 + b_4\xi^4 + b_5\xi^5$$
---------------------------------(9)

$\xi = \frac{t}{Tr} - Vn$, where a_i,b_i are i=0,1,2,3,4 and 5

Note that and for are independent of the input transition time . The solution of the SSN voltage is for

$$v_s = c_0(1-e^{-(t-Tn)/\gamma\tau r}) + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5$$
--------------------(10)

For $T_n \le t \le T_r$ where γ =(Rv_{ss} C_{Vss}+L_{Vss} f_1)/ ($R_{Vss}f_1$+1)T_r---(11)

T_n=(V_{Tn}/V_{dd})T_r=V_nT_r------------------------------(12)

These coefficients are Coefficients are

$$c_0 = A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 21A_4\gamma^5 - 120A_5\gamma^6$$
$$c_1 = A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 21A_4\gamma^4 - 120A_5\gamma^5$$
$$c_2 = A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4$$
$$c_3 = A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3 \quad c_4 = A_4\gamma + 5A_5\gamma^2,$$
$$c_5 = A_5\gamma$$ ------------------------------(13)

Here A_i for i=0,1----5 are Simultaneous switching noise results is

Ai= [(R $V_{ss}B_nV^n_{dd}$.)T_r/(Rv_{ss} C_{Vss}+L_{Vss} f_1)]a_i+ [(L $V_{ss}B_nV^n_{dd}$) /(Rv_{ss} C_{Vss}+L_{Vss} f_1)] b_i-- (14)

where and are defined in (9). The SSN voltage reaches a maximum when the input voltage completes the transition, i.e.,V_s max

$$= v_s = c_0(1-e^{-(Tr-Tn)/\gamma\tau r}) + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5$$ ------------(15)

where . The SSN voltage on a ground rail as predicted by (10) is compared to SPICE in Fig. 3 for a single CMOS inverter with m, m, and pF based on a CMOS technology. The thick solid line represents the analytical prediction and the thin line represents the results from SPICE simulations. During the time period from to , the analytical result agrees quite closely with SPICE (the error is less than 10%).

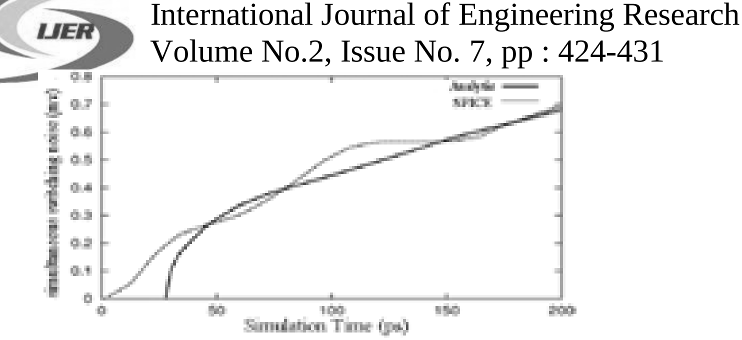


Fig. 3. SSN voltage on the ground rail for a single switching logic gate with L =2nH, R =5, C =0 :1 pF, = 29ps, and = 200 ps

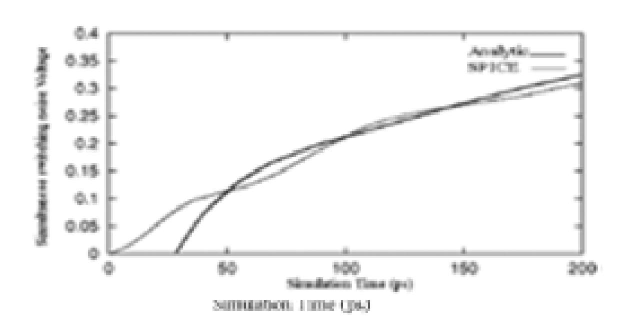


Fig. 4. SSN voltage on a ground rail for 500 simultaneously switching logic gates with L =2nH, R =5 , C =0 :1 pF, = 29ps, and = 200 ps.

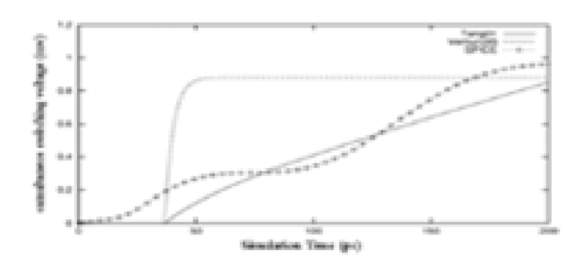


Fig. 5. The simultaneous switching voltage on a power rail with L =2nH, R =5 , C =0 :2 pF, = 39ps, and = 200 ps.

This analysis is based on a single inverter. If simultaneously switching logic gates are connected to the same ground rail, the total SSN voltage can be obtained by substituting for in (11) and (14). Note that all for are proportional to , , and . Therefore, the SSN voltage in- creases with the number of simultaneous switching logic gates , the input slew rate , and the drive current of the logic gates . The analytical prediction of the SSN voltage for five hundred simultaneously switching CMOS inverters with m, m, and pF is compared to SPICE in Fig. 4, exhibitinglessthan7%error.Duringthetimeintervalfrom to , the analytical evaluation accurately models the results from SPICE simulations. Similarly, the analytical expression for the SSN voltage on the power rail can be derived based on this same procedure. An estimate of the SSN voltage on the power rail based on the model presented in [20] is less accurate because an assumption that is close to one is made. This assumption is appropriate for short-channel NMOS transistors, but the value of in a short-channel PMOS transistor is higher, typically in the range of 1.5 to 1.8 (it is 1.68 in the target 0.5 m CMOS technology). A comparison of the SSN voltage on the power rail is shown in Fig. 5. The effect of the carrier velocity saturation on a PMOS transistor is small as compared to an NMOS transistor. There- fore, the prediction based on the model presented in [20] cannot approximate the SSN voltage on the power rail as shown in Fig. 5. Note that the analytical expression presented here accurately predicts the SSN on the power rails. The coefficients for the polynomial expansion in (9) are listed in Table I with and . The peak value of the SSN as compared to SPICE is shown in Fig. 6 with parameters m, m, andpF.ThethinlinerepresentsthepeakvalueofthepredictedSSNbased on the analytical expression described by (15). The dotted line describes the results derived from the SPICE simulations. The accuracy of the analytical prediction is within 10% as compared to SPICE. The peak SSN voltage based on (15) is compared to SPICE for different conditions, as illustrated in Tables II and III for both the ground and rails, respectively, with m, m, and the input transition timeps.Notethatthemaximumerroroftheanalyticalexpression is within 10%.

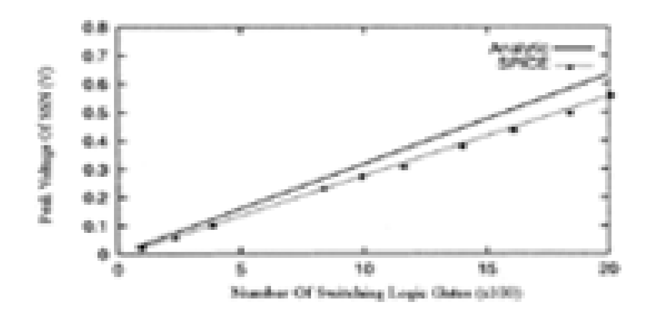


Fig. 6. The peak value of the SSN voltage with L =2nH, R =5, C =0 :1 pF, and = 200 ps.

TABLE I POLYNOMIAL EXPANSION COEFFICIENTS OF CMOS TECHNOLOGY


International Journal of Engineering Research (ISSN : 2319-6890)
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	NMOS		PMOS	
Coef.	ξ^{n_n}	$\xi^{n_n - 1}$	ξ^{n_p}	$\xi^{n_p - 1}$
0th	-0.0023	0.2391	-0.0008	0.0255
1st	0.4132	3.9601	0.0777	2.2010
2nd	1.4836	-14.9465	1.4986	-4.7503
3rd	-2.0667	31.7737	-1.2056	9.0439
4th	1.8168	-32.4443	0.9537	-8.8016
5th	-0.6502	12.5497	-0.3262	3.3138

TABLE II COMPARISON OF PEAK SSN VOLTAGE ON THE GROUND RAILS,NUM IS THE NUMBER OF SIMULTANEOUSLY SWICHING LOGIC GATES

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) ($m = 500$)			Peak SSN (V) ($m = 1000$)			Peak SSN (V) ($m = 1500$)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	0.0802	0.0762	5.2	0.159	0.150	6.0	0.236	0.218	8.2
		0.2	0.0802	0.0806	0.5	0.159	0.152	4.6	0.236	0.219	7.7
		0.3	0.0801	0.0790	0.3	0.159	0.151	5.3	0.235	0.217	8.2
	2.0	0.1	0.143	0.141	1.4	0.282	0.265	6.4	0.417	0.381	9.4
		0.2	0.143	0.137	4.3	0.282	0.263	7.2	0.417	0.380	9.7
		0.3	0.142	0.138	2.9	0.281	0.260	8.0	0.415	0.378	9.8
	4.0	0.1	0.267	0.256	4.3	0.522	0.490	6.5	0.760	0.697	9.0
		0.2	0.267	0.252	5.9	0.522	0.500	4.4	0.766	0.710	3.6
		0.3	0.267	0.286	6.6	0.521	0.530	1.7	0.765	0.742	3.5
5.0	1.0	0.1	0.104	0.102	1.9	0.206	0.197	4.6	0.300	0.284	5.6
		0.2	0.104	0.106	1.8	0.206	0.199	3.5	0.300	0.283	6.0
		0.3	0.104	0.104	0.0	0.206	0.198	4.0	0.300	0.282	6.3
	2.0	0.1	0.167	0.165	1.2	0.320	0.310	3.2	0.470	0.438	7.3
		0.2	0.167	0.162	3.1	0.320	0.308	3.9	0.470	0.436	7.7
		0.3	0.166	0.153	8.5	0.319	0.302	5.6	0.469	0.434	8.0
	4.0	0.1	0.288	0.278	3.6	0.560	0.526	6.4	0.810	0.750	8.0
		0.2	0.288	0.281	2.5	0.560	0.534	4.8	0.810	0.752	7.7
		0.3	0.287	0.308	6.5	0.559	0.567	0.1	0.810	0.790	2.5
Maximum error (%)			8.5			8.0			9.8		
Average error (%)			3.4			4.7			7.1		

TABLE III COMPARISON OF PEAK SSN VOLTAGE ON THE V RAILS,NUM IS THE NUMBER OF SIMULTANEOUSLY SWICHING LOGIC GATES

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) ($m = 500$)			Peak SSN (V) ($m = 1000$)			Peak SSN (V) ($m = 1500$)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	4.890	4.89	0.0	4.778	4.78	0.0	4.672	4.68	0.1
		0.2	4.890	4.89	0.0	4.778	4.79	0.1	4.670	4.68	0.1
		0.3	4.890	4.89	0.0	4.776	4.79	0.1	4.670	4.67	0.0
	2.0	0.1	4.794	4.81	0.3	4.599	4.63	0.6	4.412	4.47	1.3
		0.2	4.793	4.79	0.1	4.598	4.61	0.4	4.412	4.47	1.3
		0.3	4.794	4.79	0.1	4.600	4.61	0.1	4.410	4.46	1.3
	4.0	0.1	4.604	4.62	0.3	4.261	4.35	2.0	3.995	4.14	3.6
		0.2	4.604	4.63	0.4	4.260	4.36	2.0	3.994	4.13	3.6
		0.3	4.603	4.62	0.3	4.262	4.34	2.1	3.990	4.13	3.5
5.0	1.0	0.1	4.861	4.86	0.0	4.728	4.73	0.2	4.601	4.62	0.4
		0.2	4.860	4.86	0.0	4.726	4.73	0.2	4.600	4.62	0.4
		0.3	4.860	4.87	0.0	4.726	4.74	0.3	4.600	4.61	0.4
	2.0	0.1	4.770	4.78	0.2	4.554	4.59	0.8	4.351	4.42	1.6
		0.2	4.771	4.78	0.2	4.552	4.59	0.8	4.350	4.41	1.5
		0.3	4.770	4.76	0.2	4.552	4.58	0.8	4.350	4.42	1.6
	4.0	0.1	4.692	4.61	1.8	4.224	4.32	2.3	3.900	4.10	9.2
		0.2	4.690	4.61	1.7	4.220	4.32	2.3	3.905	4.11	9.3
		0.3	4.690	4.60	1.7	4.220	4.31	2.1	3.905	4.12	9.3
Maximum error (%)			1.8			2.3			9.3		
Average error (%)			0.4			1.0			2.8		

III. DISCUSSION

The dependence of the peak SSN voltage on the capacitive load is described in sub section . Circuit and layout level constraints related to the peak SSN voltage are discussed in subsec- tions and , respectively.

A. Capacitive Load

The NMOS transistor is assumed here to operate in the satu- ration region before the input transition is completed. This as- sumption depends upon the input transition time, the capacitive load, and the device transconductance. Vemuru notes in [8] that the peak value of the SSN voltage depends on the capacitive load. The time when the NMOS transistor leaves the saturation re- gion is

$T_{sat}=(C_l/B_nV_{dd+})(V_{dd}-V_{Dsat})+[(V_n+n)/1+n]T_r$----(16)

where is the drain-to-source sat- uration voltage. If , the assumption that the NMOS transistor operates solely within the saturation region before the input transition is completed is appropriate. This constraint can be expressed as(17)The dependence of the peak SSN voltage on the load ca- pacitance is shown in Fig. 7 with m and m. The right side of the vertical dashed line , i.e., Re- gion II, satisfies the constraint defined by (17). The horizontal dashed line represents the analytically predicted peak simulta- neous switching voltage. The accuracy of the analytical expres- sion in Region II is within 10%. Therefore, if the load capaci- tance and the input transition time satisfy the constraint defined by (17), the analytical prediction accurately estimates the peak SSN voltage.

$C_l \geq [(1-V_n)B_nV_{dd}^{n})/(1+n)(V_{dd}-V_{Dsat})](T_r)$-----(17)

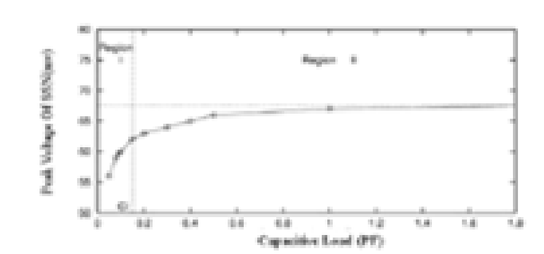
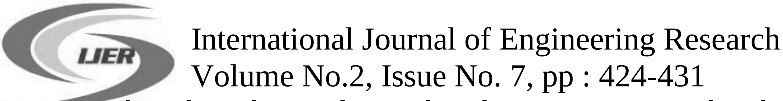


Fig.7.DependenceofthepeakSSNvoltageontheloadcapacitancewith = 200 ps.

B. Circuit-Level Constraints

The SSN voltage should be less than a target for a circuit to operate properly. Circuit design parameters, such as the input transition time , the drive current of each logic gate , and the



number of simultaneously switching logic gates connected to the same power supply rail , can be determined based on

$V_{smax}(m,B_n,T_r) \leq V_c$---------------(18)

where is defined in (15).For example, the maximum number of simultaneously switching logic gates connected to the same power supply

rail can be determined based on this constraint. Assume that V. The maximum number of switching logic gates for different conditions is shown in Fig. 8. is the condition of ps and m, is the condition of ps and m, and is the condition of ps and m and are the maximum number of switching logic gates for

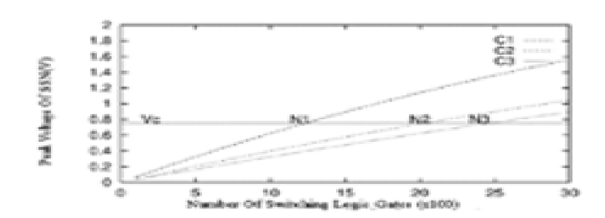


Fig. 8. The maximum number of simultaneously switching logic gates with L =2nH, R =5 , and C =0 :1 pF. V is the voltage target, C1: = 200 ps, W =3 :6 m, C2: = 400 ps, W =3 :6 m, and C3: = 200 ps, W =1 :8 m.

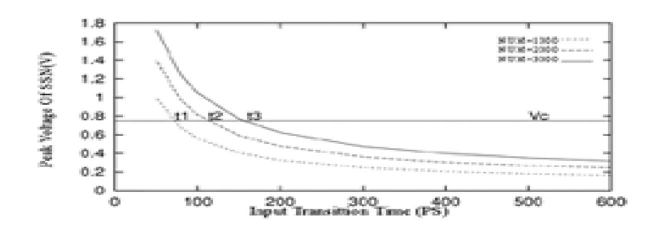


Fig. 9. Peak SSN as a function of the input transition time. Note the limiting constraints on the input transition time for different number of simultaneously switching gates, Num = 1000; 1500; and 2000

eachcase,respectively.TheonchipSSNvoltageresultsfromtheparasit icinductance of the power rails and the large current surges within a short period of time. Therefore, the peak SSN voltage increases as the input transition time decreases. The constraint of the input transition time is shown in Fig. 9 for different number of si- multaneously switching gates, e.g., 1000, 1500, and 2000 and 3000 with(1,2) nH, ,(0.1 pF,) and m(ps, ps, and ps are the limits of the input transition times for each condition, respectively. If the number of simultaneously

Fig. 10. Dependence of the peak value of the SSN on the power supply with m = 10 , L =2nH,R=5 , C =0 :1 pF, and = 200 ps.

switching logic gates increases, the input slew rate should be decreased in order to decrease the maximum SSN voltage. The peak noise values for different input transition times with nH, , and pF are listed in Table IV, note that for a very short input transition time, i.e., 20 ps, the analytical model still pro- vides an accurate estimation of the peak noise. The analytical error is within 8% as listed in Table IV. Also note that the SSN voltage is proportional to the th power of the supply voltage.Therefore, the normalized si-multaneous switching voltage is proportionaltothe , power of the supply voltage , permitting the supply voltage to be reduced in order to decrease the SSN voltage. The dashed line shown in Fig. 10 represents the normalized peak value of the SSN voltage and the solid line repre- sents the absolute value of the peak SSN.

C. Layout-Level Constraints

The peak SSN can be controlled by reducing the parasitic inductance of the power supply rails. The parasitic inductance , resistance , and capacitance of the power supply rails can be determined from the physical geometries of the layout, i.e., the width, thickness , length, and spacing of the power supply rails.Extraction of the parasitic impedance of the on-chip interconnect is currently an important research topic [20]–[22]. However, if compact models characterizing the parasitic impedance of the power supply rails are available, guidelines such as presented in (19) for designing the on-chip power distribution network can be developed. By combining both of the constraints represented by (18) and (19), the peak SSN voltage for a circuit to operate properly can be determined. The parasitic inductance of the power rails is proportional to the length of the power rails. Even though the dependence of the parasitic inductance on , , and are not available, the length of the power rail can be determined based on the par- asitic impedance per unit length. The constraint of the power rail length is shown in Fig. 11 for different conditions assuming 1500 simultaneously switching logic gates.

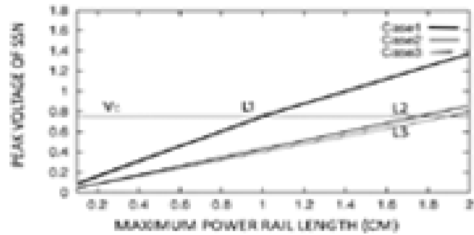


Fig. 11. Peak SSN as a function of the length of the power rails. Note the limiting constraints on the length of the power rails with 1500 simultaneously switching logic gates.

CONCLUSION : An analytical expression characterizing electromagnetic interference in sense of the SSN voltage in VDSM CMOS circuits is presented in this paper. This expression provides a method for evaluating SSN voltage at the system level. The analytically derived waveform characterizing the on-chip SSN voltage is quite close to SPICE. The predicted peak on-chip SSN voltage based on the analytical expression is within 10% as compared to SPICE. Circuit- and layout-level design constraints for the power distribution network have also been briefly discussed which will be extending the work for IR drop in dynamic power grid in vlsi/ulsi circuits by analytical em modeling or simulation .

References

i. *M. Nourani, A. Attarha. "Signal Integrity: Fault Modeling and Testing in High-Speed SoCs". Journal of Electronic Testing: Theory and Applications (JETTA), 2002, pp. 539-554.*

ii. *M. Cuviello, S. Dey, X. Bai, Y. Zhao. "Fault Modeling and Simulation for Crosstalk in System-on-Chip Interconnects". Int. Conf. on Computer Aided Design, pp. 297-303, Nov. 1999.*

iii. *W. Chen, S. Gupta, M. Breuer. "Test Generation in VLSI Circuits for Crosstalk Noise". Proc. Int. Test Conf. (ITC'98), pp. 641-650, 1998.*

iv. *P. Fang, J. Tao, J. Chen, C. Hu. "Design in Hot Carrier Reliability For High Performance Logic Applications". Proc. IEEE Custom Integrated Circuits Conf., pp. 25.1.1- 25.1.7, Oct. 1998.*

v. *Y. Leblebici. "Design Considerations for CMOS Digital Circuits with Improved Hot-Carrier Reliability". IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 1014- 1024, July 1996.*

vi. *S. Kimothi, U. Nandwani. "Uncertainty Considerations in Compliance-Testing for Electromagnetic Interference". Proc. Annual Reliability and Maintainability Symposium, pp. 265-268, 1999.*

vii. *F. Vargas, D. C. Lopes, E. Gatti, D. Prestes, D. Lupi. "On the Proposition of an EMI-Based Fault Injection Approach". Proc. 11th IEEE Int. On-Line Testing Symposium (IOLTS), pp. 207-208, 2005.*

viii. *S. Zhao, K. Roy. "Estimation of Switching Noise on Power Supply Lines in Deep Sub-Micron CMOS Circuits". Proc. Int. Conf. on VLSI Design, pp. 168-173, Jan. 2000.*

ix. *F. Vargas, D. C. Lopes, J. Chaves da Silva, D. Barros Jr. "EMI-Induced Soft-Error Rate Estimates for COTS Microprocessor". Proc. 5 th .. IEEE Latin American Test Workshop, pp.169-172, 2004.*

x. *H. Chen, L. Wang. "Design for Signal Integrity: The New Paradigm for Deep-Submicron VLSI Design". Proc. Int. Symposium on VLSI Technology, pp. 329-333, June 1997.*

xi. *D. Cho, Y. Eo, M. Seung, N. Kim, J. Wee, O. Kown, H. Park. "Interconnect Capacitance, Crosstalk and Signal Delay for 0.35µm CMOS Technology". Proc. Int. Meeting on Electron Devices, pp. 619-622, 1996.*

xii. *M. Rodriguez-Irago, J. J. Rodríguez Andina, F. Vargas, M. B. Santos, I.C Teixeira, J. P. Teixeira. "Dynamic Fault Test and Diagnosis in Digital Systems Using Multiple Clock Schemes and Multi-VDD Test". Proc. 11th IEEE Int. On-Line Testing Symposium (IOLTS), pp. 281-286, 2005.*

xiii. *D. W. Dobberpuhl et al., "A 200-MHz 64-bit dual-issue CMOS micro-processor," IEEE J. Solid-State Circuits, vol. 27, pp. 1555–1565, Nov. 1992.*

xiv. *W. J. Bowhill et al., "Circuit implementation of a 300-MHz 64-bit second-generation CMOS alpha CPU," Digital Tech. J., vol. 7, no. 1, pp. 100–118, 1995.*

xv. *P. E. Gronowski et al., "High-performance microprocessor design," IEEE J. Solid-State Circuits, vol. 33, pp. 676–686, May 1998.*

xvi. *G. Katopis, "I noise specification for a high performance computer machine," Proc. IEEE, vol. 73, pp. 1405–1415, Sept. 1985.*

xvii. *P. Larsson, "di=dt noise in CMOS integrated circuits," Analog Inte-grated Circuits Signal Processing, vol. 14, no. 1/2, pp. 113–129, Sept. 1997.*

xviii. *A. J. Rainal, "Computing inductive noise of CMOS drivers," IEEE Trans. Components, Packaging, Manuf. Technol.—Part B, vol. 19, pp. 789–802, Nov. 1996.*

xix. *A. Vaidyanath, B. Thoroddsen, and J. L. Prince, "Effect of CMOS driver loading conditionson simultaneous switchingnoise," IEEE Trans.Com-ponents, Packaging, Manuf. Technol.—Part B, vol. 17, pp. 480–485, Nov. 1994.*

xx. *S. R. Vemuru, "Accurate simultaneous switching noise estimation including velocity-saturation effects," IEEE Trans. Components, Packaging, Manuf. Technol.—Part B, vol. 19, pp. 344–349, May 1996.*

xxi. *Y. Yang and J. R. Brews, "Design for velocity saturated, short-channel CMOS drivers with simultaneous switching noise and switching time considerations," IEEE J. Solid-State Circuits, vol. 31, pp. 1357–1361, Sept. 1996.*

xxii. *"Design Sciences Tab: Physical Design Task Force Report," Tech. Rep., Semiconductor Research Corporation Physical Design Task Force, Semiconductor Research Corp., New Durham, NC, 1997.*

xxiii. *"The National Technology Roadmap for Semiconductor," Semicon-ductor Industry Assoc., San Jose, CA, 1994.*

xxiv. *"The National Technology Roadmap for Semiconductors," Semicon-ductor Industry Assoc., San Jose, CA, 1997.*

xxv. *L.-R. Zheng and H. Tenhunen, "Effective power and ground distribution scheme for deep submicron high speed VLSI circuits," in Proc. IEEE Int. Symp. Circuits and Systems, Orlando, FL, May 1999, pp. 537–540.*

xxvi. *S. R. Vemuru, "Effects of simultaneous switching noise on the tapered buffer design," IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 5, pp. 290–300, Sept. 1997.*

xxvii. *E. G. Friedman, Clock Distribution Networks in VLSI Circuits and Sys- tems. Piscataway, NJ: IEEE Press, 1995.*

xxviii. *High Performance Clock Distribution Networks. Norwell, MA: Kluwer, 1997.*

xxix. *T. Sakurai and A. R. Newton, "A simple MOSFET model for circuit analysis," IEEE Trans. Electron Devices, vol. 38, pp. 887–894, Apr. 1991.*

xxx. *H. Shichman and D. A. Hodges, "Modeling and simulation of insu-lated-gate field-effect transistor switching circuit," IEEE J. Solid-State Circuits, vol. SC-3, pp. 285–289, Sept. 1968.*

xxxi. *N. Hedenstierna and K. O. Jeppson, "CMOS circuits speed and buffer optimization," IEEE Trans. Comput.-Aided Design Integrated Circuits Syst., vol. CAD-6, pp. 270–280, Mar. 1987.*

xxxii. *D. A. Priore, "Inductance on Silicon for sub-micron CMOS VLSI," in Proc. IEEE Symp. VLSI Circuits, Kyoto, Japan, May 1993, pp. 17–18.*

xxxiii. *N. Delorme, M. Belleville, and J. Chilo, "Inductance and capacitance formulas for VLSI interconnects," Inst. Elect. Eng. Electron. Lett., vol. 32, no. 5, pp. 996–997, May 1996.*

xxxiv. *S. Wong et al., "Interconnect capacitance models for VLSI circuits," Solid-State Electron., vol. 42, no. 6, pp. 969–977, June 1998.*